TUNING METHODS FOR CHARACTERIZING COMPLICATED FUNCTIONALITY CIRCUITS

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Abstract – *In this work methods are presented for characterising complicated functionality blocks (CF-blocks). Various methods of reduction is being proposed including: removing parts of the circuit which don't have any significant impact on the calculations, based on the information about the structure of CF-blocks, deleting not active parts of the circuit, deleting parts of the circuit based on automatically decomposing circuit into sub-circuit of components connected with direct current (Direct Current Connected Components = DCCC). Another proposed method is based on reducing the number of calculations in electrical level by finding and reducing the repeated calculations for various cases of inputs signals and output loads.*

1. INTRODUCTION

Characterization of logic library is a process of myriad simulations in circuit level for different technological and schematically parameters. Usually simulations are being performed by means of precise circuit simulators (like HSpice). The characterization process is very tough and usually requires from several weeks to several months of computer time. For parameterized CF blocks the number of simulations can be much bigger than for usual blocks, this is connected with the fact that calculations of various CF blocks with different parameters is needed and for each of that configuration separate calculations for each PVT (Process Voltage Temperature) is needed. In contemporary to that only one calculation with given configuration, with big number of transistors and RC-chains, can be characterised, depending on given precision, from several hours to days in modern computers. As a result of this an issue is rising for decreasing the time of calculations by keeping the same correctness. In this work the speed of characterisation is being decreased by two proposed methods:

1) Reduction the circuit by deleting not active or negligible parts of that circuit keeping the same load on the boundaries of cut fragments. This method can be divided into 3 different sub-methods which can be combined or mixed among each other:

a) Deleting the parts of the circuit which don't have any impact on calculations, this can be done based on information from developers about the structure of parameterised CF-block.

b) Deleting not active parts of the circuit. Such parts can be figured out based on initial simulations which are using simplified models and tuned calculations methods in the cost of deceased correctness.

c) Deleting non-significant for measurements parts of the circuit (even active) based on dividing the circuit into DCCC [1]-[2].

2) Increasing the speed of characterization - decreasing the number of calculations in the circuit during simulation by figuring out and removing the repeated calculations. In this work for decreasing the number of calculations proposed to use initial analyse of timing characterisation dependency on input edges and output loads.

2. DECOMPOSING CIRCUIT INTO SUB-CIRCUIT OF ELEMENTS CONNECTED WITH DIRECT CURRENT

For automatically reduction the initial analyse of the structure of CF-block is needed. The proposed method of structural analyse is based on dividing circuit into DCCC by using the representation of the circuit as a directed graph [3].

The MOS-graph will be called non-oriented graph G=(V, E), built in based on MOS circuit keeping following rules: to each node of the MOS circuit correspond one and only one vertex of the graph, to each element of the graph correspond one and only one edge of the G=(V, E) graph, connected vertexes correspond to nodes of elements.

In general MOS-graph can have several nodes logically equivalent to ground "0" and several nodes logically equivalent to supply pins "1". The group of those nodes with their connected edges will be called correspondingly chain of ground and chain of supply. In a simple case each of the chains of ground and supply consist of one node and many empty edges. Figuring out the sub-graphs of ground and supply allow to divide the MOS graph into many not meeting to each other connected components.

Lets assign $E_R(G)$the sub-group of edges (V_0,V_1) MOS graph describing the pair of logically equivalent nodes i.e. logic equation like $f_{V0}= f_{V1}$. In most cases such edges form the resistors.

Chain of ground of MOS graph G=(V, E) will be called sub-graph $G_0=(V_0, E_0)$ of graph G=(V, E) which was recursively built with following rules:

1) The nodes of ground, assigned with 0, belong to the chain of ground $v_0 \in V_0$.

2) If $x \in V_0$ and $(x,y) \in E_R(G)$, then $y \in V_0$ and $(x,y) \in E_R(G)$.

3) $v_0 \in V_0$, $(x,y) \in E_0$ – if and only if they can be added to the chain of ground based on 1 and 2 rules.

Chain of supply of MOS graph G=(V,E) will be called sub-graph $G_1=(V_1,E_1)$ of graph G=(V,E) which was recursively built with the same rules as the chain of ground, just instead of ground supply needs to be take. In a simple case each of the chains of ground and supply consist of one boundary of vertexes without edges.

Lets G=(V,E) MOS graph, $G_0=(V_0,E_0)$ ground chain of G graph, $G_1=(V_1,E_1)$ supply chain of G graph and $e_0=(x_0,y_0)$, $e_0 \in E \setminus (E_0 \cup E_1)$ – edge of the graph G=(V,E), not included in the chain of ground. In that case the sub-circuit of elements, connected with direct current for the given e_0 edge will be called sub-graph $G_D(e_0)=(V_D(e_0),E_D(e_0))$ of G=(V,E) graph, which meets the following conditions

1) The given edge belongs to DCCC $e_0 \in E_D(e_0)$;

2) The nodes of all graphs, included in DCCC, belong to DCCC i.e. if $(x,y) \in E_D(e_0)$, then $x \in V_D(e_0)$, $y \in V_D(e_0)$,

3) For all nodes of DCCC, except the supply and ground nodes, all edges belong to DCCC i.e. if $x \in V_D(e_0) \setminus (V_0 \cup V_1)$ and $(x,y) \in V$ then $(x,y) \in V_D(e_0)$.

4) $x \in V_D(e_0)$, $(x,y) \in E_D(e_0)$ – if and only if they can be added to DCCC based on (1),(2),(3) rules.

The standard MOS element – it is one DCCC, the simplest example of DCCC is a buffer consisting of two inverters as it is shown in fig. 1.

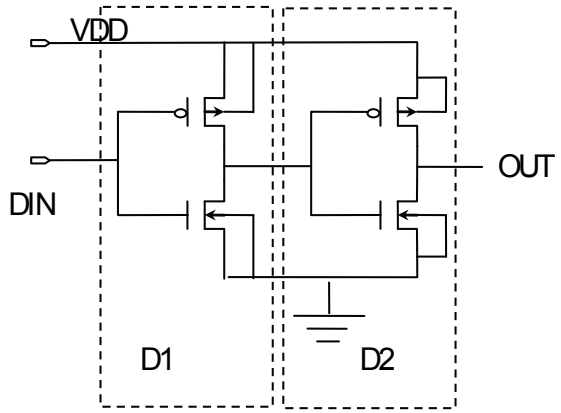

Fig.1. *Deviding the buffer into two DCCC (D1, D2)*

More complicated types of DCCC are shown in figures 2 and 3. In figure 2 a simple CMOS switch was divided into three DCCC D1, D2 and D3. And in the figure 3 the same CMOS switch was used to build a CMOS trigger, the trigger was divided into four DCCC.

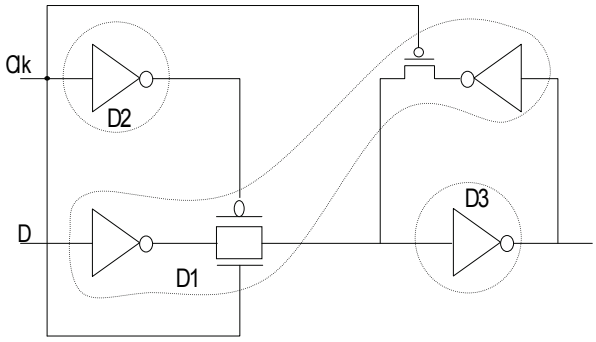

Fig.2. *DCCC decomposition of CMOS switch (D1, D2,D3)*

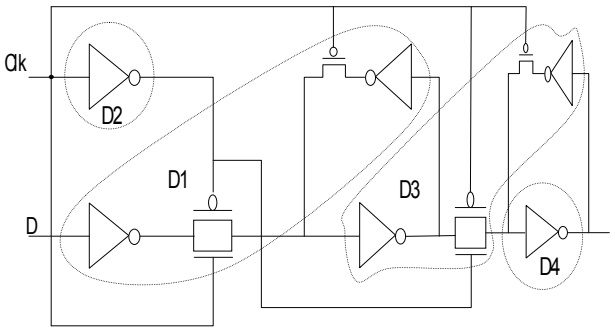

Fig.3. *DCCC decomposition of CMOS trigger*

The important points of discussion in this paper are: a) the decomposition of DCCC can be performed for any circuit which is given in transistor level, b) DCCC is the analogous of standard elements, c) DCCC guarantees analyze of transferring the signal from the inputs of DCCC to its outputs.

3. REDUCTION OF THE CIRCUIT BASED ON METHOD OF COSINUSES.

The specification for characterization usually consists of two parts: the hierarchicla spice netlist of the file and calculaiton specification (CKT-file) which continas: the settings of simulator, PVT corners, input signals and inputs signals parameters range, the set of measures that needs to be done. The algorithm of reduction is following:

1) Divide the circuit into DCCC and sort DCCC with the levels from inputs to outputs. During the sorting process the cycles will be broken up if there are such in the circuit.

2) Analysing the given measures in CKT file. Foreach node of cell from measures find the DCCC to which it belongs and mark it with the flag „isNeeded“.

3) Moving from outputs to inputs mark all DCCC with the flag „isNeeded“ in case when there exist connection between the analysing DCCC and the DCCC which is already marked as „isNeeded“.

4) For creating the circuit which is equivalient to initial one, in the boundries of active DCCC the load capacitance needs to be assigned. Because of specifications of DCCC decomposition beyond the bordres of DCCC in the first line the transistors exist, which are connected with their drain. The amount of elements whcih are left outside the DCCC borders impact on the correctness of calculations. In order to give to user capability to choose between the speed and corectness the depth parameter can be induced, which shows the number of elements which were left out of the DCCC borders.

4. REDUCTION OF THE CIRCUIT BY USING THE RESULTS OF FAST CIRCUIT SIMULATOR

The main idealogy of this method is to exclude from consideration all elements on which nodes there are not switching and replace that nodes in which the active elements with fixed values are connected (VDD or GND).

As the initial calculations doesn’t need much preciseness then for that calculation can be useed the following simplification

1) Simple model of transistors

2) The fastest calculaiton method. The experiments have shown the fast calculaitons can be one or even hundread times faster than the calculaitons with all models and big preciseness.

By correctly using the simulator [4] special file can be received as an output which contains the list of non-active nodes. The node is called not active if the votage in it is less than some value, and the statical values of all nodes in some moment of time. If the element in not active than it can be removen from the circuit without having any impact on measurements.

5. ANALYSE OF DEPENDANCY CHARACTERISTIC ON INPUT FRONTS AND LOADS

The main result of characterization of CF-block is a file in Liberty [5] format. The characters like setup, hold and delays are given in that file with one or two dimensional matrixes

Let's analyse the matrix of CLK-Q delay signal. That table depends on two parameters: input front width and output load in Q. In case of standard cells the calculation of that matrix is done by performing N*M simulations of the circuit with N different input fronts and M output loads. However for CF-blocks consisting of many levels of DCCC that method can be optimized

1) For each CF-blocks, on which the measurements are being performed, the corresponding DCCC is being found and it is copied M times. In the input of each DCCC the followers are being connected with the nodes of original DCCC. And a capacity is being copied for the outputs of each copied DCCC. The measure is being copied for the outputs of each copied DCCC. Because of negligible size of DCCC in outputs, in comparison with the original circuit, the simulation increasing time is little whereas the number of re-simulations is decreasing M times which give significant speed-up to characterization.

2) For each clock input to the circuit the DCCCs of that input are being found, no deeper that 4 level and that part of that scheme is being copied N times in the input with different fronts. On each DCCC located in level 3 the measure is being putted on CLK. For each measure the maximum difference is being calculated compared with the original scheme measure. The difference is being used during construction the final table of measurements.

6. SETUP AND HOLD TIME ACCELERATED ANALYSIS

One of the possible options to decrease the number of calculations in the scheme is an indirect measurement of required parameter. Some measurements, like setup and hold times in synchronous CF-blocks are being performed by direct methods with the help of zero order optimization solutions.

In the first stage it is required to set the list of circuit active chains from data to clock signal switch. In this method it is necessary to use setup and hold times that will guarantee circuit correct performance and after allocate all logic elements (DCCC) which are controlled two signals simultaneously. Assume that for proper function of time event method is requires that for all DCCC data signal is settled before clock signal active edge, besides it is required to take into account other elements which don't considered as DCCC elements, that have the function of logic gate. In order to shift the data signal to clock taking into account time-even approach needs to calculate all delay from data signal to clock and after find the minimal one. Delay calculation is following:

Setup = (Delay (d-clock) –Delay (min))

For setup time calculation practically the same solution is used. Firstly lets clarify that memory element in simple case is two DCCC with feedback, whereas in real circuit the feedback may pass through additional DCCC. Feedback loop depth is being defined by users. For locating all active chains till fist memory element second method is used. After, as in previous case, delays from clock to data signal negedge are calculated. In respect to data signal negedge there is minimal hold time calculated by

Hold = (Delay (clock-d)-Delay (min_reduced)

The indirectly received results check is performed by circuit post-verification for operability with all set of received values for all input pins.

7. EXPERIMENTAL RESULTS

A program was developed based on theoretical research which has all suggested methods included in it. Testing was performed on real memory circuits (a certain case of parameterized CF-block) with different configurations (from the smallest to the biggest), with different types (Single Port, Double Port and ROM). For testing purposes Hspice simulator was used. For accuracy measurements slow option was used (slow option for the highest measurements results) and for accelerating measurements Normal option was used (fast option for the medium measurements results). Normal option is usually used for characterisation. Maximum error rate in method of cosiness was about 6% (for calculations greater than 1ns) and about 48ps (for calculations less than 1ns). The most acceleration boost was reported in big configurations where calculation time was about 2-3 time compared to the initial one.

Testing results with cosiness methods are brought in Table 1. *Time of calculation of all and reduced circuits Results and* Table 2. *Error rate*. In first column of 1, 2 tables the memory circuit names can be seems, access calculations types are marked (1) and setup/hold calculation time is marked (2). In second column of table (1) the calculation time of overall circuit is decreased three times.

Tabe 1. *Time of calculationof all and reduced circuits*

Configuration	Time of calculation		Speed-up(X)
Sp_00032x004m04b1	86.26	62.13	1.39
Sp_02560x048m16b1	4893.64	282.72	16.60
Sp_16384x072m08b4	141.79	254.02	5.19
Dp_000116x004m02b1	78.29	68.69	1.14

Tabe 2. *Error rate*

Configuration	Time of calculation	
Sp_00032x004m04b1	0.90%	-3.22ps
Sp_02560x048m16b1	-4.03%	-46.47ps
Sp_16384x072m08b4	-5.08%	-38.68ps
Dp_000116x004m02b1	1.11%	-5.83ps

8. CONCLUSION

As can be seen from the experimental results the proposed methods gives us a capability to decrease the time of calculation, by keeping the same preciseness for the CF-blocks.

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